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Description

[DYNAMIC RANDOM ACCESS MEMORY CELL AND FABRICATION THEREOF]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation-in-part (CIP) application of U.S. Patent Application of Serial No. 10/210,031 filed August 02, 2002, the entire contents thereof are incorporated herein for reference.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] This invention pertains in general to semiconductor devices, and, more particularly, to memory cells for a dynamic random access memory (DRAM) and processes for manufacturing the same.

[0004] Description of the Related Art

[0005] In the semiconductor industry, DRAM is one of the most important integrated circuits, which motivates continuing research and development. There is a continuing effort to

increase the storage capacity, improve the writing and reading speed, and decrease the device dimensions of a DRAM cell. A DRAM cell generally includes a transistor and a capacitor operated by the transistor. Conventionally, the design of a DRAM cell can be divided into three types, namely, planar, stacked-capacitor and trench. In the planar design, the transistor and capacitor of a cell are produced as planar components. In the stacked-capacitor design, the capacitor of a cell is disposed above the transistor. In the trench design, the transistor is disposed on the surface of a substrate, and the capacitor is disposed in a trench formed in the substrate.

[0006] The process of forming a trench, however, requires an accurate alignment of mask work. For deep sub-micron semiconductor devices, a deep trench may have a length-to-diameter aspect ratio of 40:1. Typically, capacitors are formed in the deep and narrow trenches by depositing a dielectric layer on the trench walls and filling the trench with a doped polysilicon layer. As the aspect ratio becomes higher, for example, exceeds 20:1, the trench becomes more difficult to fill.

SUMMARY OF INVENTION

[0007] In view of the foregoing, on aspect of this invention is to

provide a dynamic random access memory (DRAM) cell that has a capacitor formed on the sidewall of a semiconductor pillar to eliminate the trench-filling problem in the prior art and to increase capacitor surface area.

[0008] Another aspect of this invention is to provide a DRAM array based on the DRAM cell structure of this invention. The DRAM array can have a higher degree of integration because vertical transistors are formed in the memory cells.

[0009] Still, another aspect of this invention is to provide a method for fabricating a DRAM array, so as to eliminate the trench-filling problem in the prior art and increase the integration of DRAM devices.

[0010] The DRAM cell of this invention includes a semiconductor pillar formed on a substrate, a capacitor formed on the lower portion of the sidewall of the pillar, and a vertical transistor formed on the upper portion of the sidewall of the pillar. The capacitor includes a first plate in the lower portion of the sidewall of the pillar, a dielectric layer covering the lower portion of the sidewall of the pillar, and a second plate covering the dielectric layer. The vertical transistor includes a first doped region, a second doped region, a gate and a gate insulating layer. The first doped

region is located in the sidewall, and is coupled to the second plate of the capacitor. The second doped region is located in the top portion of the pillar. The gate is disposed on the sidewall of the pillar between the first and the second doped regions. The gate insulating layer is disposed between the sidewall of the pillar and the gate.

[0011] The DRAM array of this invention includes rows and columns of the aforementioned memory cells of this invention, a plurality of bit lines and a plurality of word lines. The memory cells are disposed on a semiconductor substrate, and have the same structure mentioned above. The second doped regions of the memory cells in one row are coupled to a bit line, and the gates of the memory cells in one column are coupled to a word line.

[0012] The method for fabricating a DRAM array of this invention is described as follows. A semiconductor substrate is patterned to form rows and columns of pillars thereon, and then a capacitor is formed on the lower portion of the sidewall of each pillar. The spaces between the pillars are partially filled with a first insulating material to cover the capacitors. A gate structure of a transistor is formed on the sidewall of each pillar above the first insulating layer, including a gate electrode and a gate insulating layer be-

tween the pillar and the gate electrode. A first doped region of a transistor is formed in the sidewall of each pillar coupling with the capacitor formed on the same pillar. A second doped region of a transistor is formed in a top portion of each pillar. After the transistor fabrication is completed, the spaces between the pillars are filled with a second insulating material to cover the transistors. A plurality of bit lines is then formed over the substrate, wherein each bit line is electrically connected to the second doped regions of the transistors in one row. In addition, a plurality of word lines is formed over the substrate, wherein each word line is coupled with the gates of the transistors in one column through gate contacts.

[0013] Since the capacitor in a DRAM cell of this invention is formed around a semiconductor pillar, but not in a deep trench, the trench-filling problem in the prior art due to the high aspect ratio of deep trenches is thus obviated. Meanwhile, the surface area of the capacitor is quite large because the capacitor can be formed on all sides of the pillar, i.e., all sides of the memory cell.

[0014] Moreover, since the transistor of a DRAM cell of this invention is formed with a vertical structure, the lateral area occupied by a memory cell can be significantly reduced to

remarkably increase the integration of a DRAM array. In other words, the DRAM array of this invention can have a higher degree of integration.

[0015] Furthermore, since a capacitor is formed around a semiconductor pillar in the method for fabricating a DRAM array of this invention, the trench-filling problem in the prior art is precluded. Therefore, the quality of the storage capacitors can be improved.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0017] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0018] FIGs. 1-16 illustrate a process flow of fabricating a DRAM array according to a preferred embodiment of this invention, wherein FIGs. 1-6 illustrate the process flow of forming the capacitors of the DRAM array, FIGs. 7-12 il-

lustrate the process flow of forming the vertical transistors of the DRAM array, and FIGs. 13-16 illustrate the subsequent steps including the fabrications of the bit lines and the word lines.

[0019] FIGs. 2A-6A illustrate another process flow of forming the capacitors of the DRAM array according to the preferred embodiment of this invention in a cross-sectional view.

[0020] FIGs. 7A-10A illustrate another process flow of forming the gate structures of the vertical transistors of the DRAM array according to the preferred embodiment of this invention.

DETAILED DESCRIPTION

[0021] FIGs. 1-16 illustrate a process flow of fabricating a DRAM array according to a preferred embodiment of this invention. FIG. 1 clearly presents the array arrangement in a perspective view, FIGs. 2-9, 11-13 and 16(a) are cross-sectional view along line I-I" in FIG. 1, while FIG. 16(b) is another cross-sectional view and FIGs. 10, 14 and 15 are top views.

[0022] More specifically, FIGs. 1-6 illustrate the process flow of forming the capacitors of the DRAM array, FIGs. 7-12 illustrate the process flow of forming the transistors of the DRAM array, and FIGs. 13-16 illustrate the subsequent

steps including the fabrications of the bit lines and the word lines.

[0023] *Fabrication of Capacitors*

[0024] Referring to FIG. 1, a semiconductor substrate 100, such as a P-doped silicon substrate, is provided, and a pad oxide layer 102 and a patterned mask layer 104 are further formed on the substrate 100. The patterned mask layer 104 includes rows and columns of rectangular (or square) blocks, and is formed with a material such as silicon nitride (SiN). The substrate 100 is then etched using the patterned mask layer 104 as a mask to form rows and columns of semiconductor pillars 110. It is noted that each block of the patterned mask layer 104 may alternatively have a round shape, an elliptical shape or another polygonal shape when viewed from the top, even though the top view of the patterned mask layer 104 as shown in the figure has a rectangular (or square) shape. In the alternative cases, however, a pillar 110 is shaped as a cylinder, an elliptical cylinder, or a corresponding polygonal pillar.

[0025] Moreover, it is particularly noted that a semiconductor pillar 110 and the portion of the mask layer 104 thereon together are sometimes referred to as a pillar 110 in the

descriptions of the specification hereinafter for convenience.

[0026] Referring to FIG. 1 again, a common electrode 112 of the subsequently formed storage capacitors is formed in the lower portion of the sidewall of each pillar 110 and in the surface layer of the substrate 100 with a doping method. The doping method includes the following steps, for example. An arsenic-doped silicon oxide layer (not shown) is formed between the pillars 110, having a predetermined depth. The arsenic-doped silicon oxide layer can be formed by, for example, depositing silicon oxide with in-situ arsenic doping over the substrate 100 to fill the spaces between the pillars 110 and etching back the arsenic-doped silicon oxide until its depth is increased to the predetermined one. Alternately, the arsenic-doped silicon oxide layer can be formed covering the lower portion of pillar sidewall through photoresist coating and etching back process to define the predetermined depth. After the arsenic-doped silicon oxide layer is covered with an undoped silicon oxide layer, a thermal process is performed to thermally driving some arsenic atoms from the arsenic-doped silicon oxide layer into the contacting surface layers of the semiconductor pillars 110 and the sur-

face layer of the bottom substrate 100.

[0027] The subsequent steps for completing the fabrication of the capacitors are illustrated in FIGs. 2-6, wherein Figures 2-6 are cross-sectional views along the cutting line I-I" in FIG. 1.

[0028] Referring to FIG. 2, a conformal dielectric layer 114 is formed on the substrate 100 and the pillars 110. The conformal dielectric layer 114 is preferably an oxide/nitride/oxide (ONO) or nitride/oxide (NO) composite layer as a capacitor dielectric layer. A conductive layer 116 is then formed between the pillars 110 with a top depth approximately the same as (or lower than) that of the common electrode 112. The conductive layer 116 is formed with a material such as N^+-doped polysilicon, and can be formed by, for example, depositing polysilicon with in-situ doping over the substrate 100 to fill the spaces between the pillars 110 and etching back the doped polysilicon to a predetermined depth.

[0029] Referring to FIG. 3, the dielectric layer 114 exposed by the conductive layer 116 is removed. The method for removing the exposed dielectric layer 114 may include a wet etching process. When the dielectric layer 114 is an ONO composite layer comprising a top oxide layer, a nitride

layer and a bottom oxide layer, for example, dilute hydrofluoric acid, phosphoric acid and dilute hydrofluoric acid can be used in sequence to remove the exposed top oxide layer, the exposed nitride layer and the exposed bottom oxide layer, respectively.

[0030] Referring to FIG. 4, an insulating spacer 118 is formed on the sidewall of each pillar 110 above the conductive layer 116. The insulating spacer 118 is composed of a material such as silicon oxide, and is formed with chemical vapor deposition (CVD) and subsequent anisotropic etching, for example. It is noted that although the insulating spacer 118 is shown to form on two sides of the corresponding pillar 110 in the cross-sectional view, it actually surrounds the pillar 110. A conductive layer 120 is then formed between the pillars overlying the conductive layer 116 and covering a lower portion of each insulating spacer 118. The conductive layer 120 is composed of a material such as N^+-doped polysilicon, and can be formed by, for example, depositing polysilicon over the substrate 100 with in-situ doping and then etching back the doped polysilicon to the predetermined depth.

[0031] Referring to FIG. 5, the insulating spacer 118 on each pillar 110 exposed by the conductive layer 120 is removed

to form a collar insulating layer 118a surrounding the pillar 110. Another conductive layer 122 is formed between the pillars 110 overlying the collar insulating layer 118a and the conductive layer 120. The conductive layer 122 is formed with a material such as N^+-doped polysilicon, and can be formed by, for example, depositing polysilicon over the substrate 100 with in-situ doping and then etching back the doped polysilicon to the predetermined depth. Thereafter, a mask spacer 124 is formed on the sidewall of each pillar above the conductive layer 122, having a thickness larger than that of the collar insulating layer 118a. The mask spacer 124 is for defining an upper electrode of a capacitor, as described below.

[0032] Referring to FIGs. 5 and 6 simultaneously, the three conductive layers 122, 120 and 116 are sequentially etched using the mask spacers 124 as a mask to form an upper electrode 126 on the lower sidewall of each pillar 110. It is noted that the remaining conductive layer 122, i.e., the top portion of the upper electrode 126, directly contacts with the sidewall of the semiconductor pillar 110. The upper electrode 126, the dielectric layer 114 and the common electrode 112 together constitute a capacitor 127. Thereafter, the mask spacers 124 are removed, and an in-

sulating layer 128 is filled between the pillars 110 to cover all capacitors 127. The insulating layer 128 is formed with a material such as silicon oxide, and can be formed by, for example, depositing silicon oxide over the substrate 100 and then etching back the silicon oxide to the predetermined depth.

[0033] The capacitor 127 may also be formed with other methods. For example, FIGs. 2A-6A illustrate another process flow of forming the capacitors of the DRAM array in a cross-sectional view.

[0034] Referring to FIG. 2A, after the pillars 110 are defined and the common electrode 112 is formed, a conformal dielectric layer 114 is formed over the substrate 100. A conductive spacer 216 is then formed on the sidewall of each pillar 110. An insulating layer 218 is formed between the pillars 110 with a top depth approximately the same as (or lower than) that of the common electrode 112. The insulating layer 218 is composed of a material such as silicon oxide, and can be formed by, for example, depositing silicon oxide over the substrate 100 and then etching back the silicon oxide to the predetermined depth.

[0035] Referring to FIG. 3A, the conductive spacer 216 and the conformal dielectric layer 114 exposed by the insulating

layer 218 are removed. The remaining conductive spacer 216a is a first part of the upper electrode that will be completed later.

[0036] Referring to FIG. 4A, an insulating spacer 118 is formed on the sidewall of each pillar 110 above the insulating layer 218. A conductive layer 120 is then formed between the pillars 110 overlying the conductive layer 216a and the insulating layer 218 and covering a lower portion of the insulating spacer 118.

[0037] Referring to FIG. 5A, the insulating spacer 118 on each pillar 110 exposed by the conductive layer 120 is removed to form a collar insulating layer 118a surrounding the pillar 110. Another conductive layer 122 is formed between the pillars 110 overlying the collar insulating layer 118a and the conductive layer 120. Thereafter, a mask spacer 124 is formed on the sidewall of each pillar 110 above the conductive layer 122, having a thickness larger than that of the collar insulating layer 118a. The mask spacer 124 is for defining an upper electrode of a capacitor, as described below.

[0038] Referring to FIGs. 5A and 6A simultaneously, the two conductive layers 122 and 120 are sequentially etched using the mask spacers 124 as a mask. The remaining conduc-

tive layers 122 and 120 and the conductive spacer 216a formed previously together form an upper electrode 126, wherein the conductive layer 122, i.e., the top portion of the upper electrode 126, directly contacts with the sidewall of the semiconductor pillar 110. The upper electrode 126, the dielectric layer 114 and the common electrode 112 together form a capacitor 127. Thereafter, the mask spacers 124 are removed, and an insulating layer 128 is filled between the pillars 110 covering the remaining conductive layers 122 and 120 and the insulating layer 218.

[0039] Moreover, in the two methods for forming a capacitor around each pillar, some modifications or variations on, for example, the material and the fabrication method of each layer and the fabrication sequence of the layers, are also possible within the scope of this invention.

[0040] *Fabrication of Transistors*

[0041] Fabrication of Gate Structures

[0042] Referring to FIG. 7, after the insulating layer 128 is formed to isolate the upper electrode 126, a gate insulating layer 130 is formed on the exposed sidewall of each semiconductor pillar 110. The gate insulating layer 130 is, for example, a thin silicon oxide layer or a thin oxide/ni-

tride layer, and may be formed with a thermal oxidation process or a thermal oxidation-nitridation process. A conductive layer 132 is then formed between the pillars 110 overlying the insulating layer 128 and covering the lower portion of the gate insulating layer 130. The conductive layer 132 is composed of a material such as N^+-doped polysilicon, and can be formed by, for example, depositing polysilicon over the substrate 100 with in-situ doping and etching back the doped polysilicon to the predetermined depth.

[0043] Referring to FIG. 8, a mask spacer 134 is formed on the sidewall of each pillar 110 above the conductive layer 132. The mask spacer 134 is for defining a gate later, and is formed with an insulating material such as silicon oxide.

[0044] Refer to FIGs. 9-10, wherein FIG. 10 is a top view of the resulting structure after the following steps, and FIG. 9 is a cross-sectional view of the resulting structure in FIG. 10 along line IX-IX'. A patterned mask layer 136, such as a patterned photoresist layer, is formed over the substrate 100. The patterned mask layer 136 includes parallel linear patterns 1361, wherein each linear pattern 1361 covers the pillars 110 in one column and the conductive layer 132 between the pillars of the same column. The conduc-

tive layer 132 is then etched using the mask spacers 134 and the patterned mask layer 136 as a mask to form a gate 132a on the sidewall of each pillar 110. A mask spacer 134 ensures the corresponding gate 132a to surround the corresponding pillar 110 even if misalignments of the patterned mask layer 136 has occurred. The gates 132a on the sidewalls of the pillars 110 in one column are connected via the remaining conductive layer 132a between the pillars 110 of the same column to be a gate line 132a (dotted region), which can directly serve as a word line. However, another low-resistance conductive line can be further formed overlying and electrically connecting with the gate line 132a to reduce the resistance, as described later.

[0045] The gate structure that includes the gate insulating layer 130 and the gate 132a may also be formed with other methods. For example, FIGs. 7A-10A illustrate another process flow of forming the gate structures of the vertical transistors of the DRAM array.

[0046] Referring to FIG. 7A, after the insulating layer 128 is formed to isolate the upper electrode 126, a conformal conductive layer 232, such as a conformal N^+-doped polysilicon layer, is formed over the substrate 100. A

mask layer 234 is then form between the pillars 110 to cover the bottom portion of the conductive layer 232 on the insulating layer 128, the mask layer 234 having a thickness sufficient to resist the anisotropic etching plasma for defining the gate lines, as described later. The mask layer 234 is formed with a material such as silicon oxide, and can be formed by, for example, depositing silicon oxide on the conductive layer 232 to fill the spaces between the pillars 110 and then etching back the silicon oxide to the predetermined depth.

[0047] Referring to FIGs. 8A and 10A, wherein FIG. 10A is a top view of the resulting structure after the following steps, and FIG. 8A is a cross-sectional view of the resulting structure in FIG. 10A along line VIII-VIII". A patterned mask layer 236 is formed over the substrate 100, including parallel linear patterns 2361, wherein each linear pattern 2361 covers the conductive layer 232 on the tops of the pillars 110 in one column and the conductive layer 232 and the mask layer 234 between the pillars 110 of the same column. The mask layer 234 exposed by the patterned mask layer 236 is then removed to expose a portion of the conductive layer 232 between every two columns of pillars 110.

[0048] Referring to FIG. 9A as well as FIGs. 8A and 10A, the mask layer 236 is removed to expose the remaining mask layer 234 between the pillars 110 in each column and the conductive layer 232 not covered by the remaining mask layer 234. The conductive layer 232 is then anisotropically etched using the mask layer 234 as a mask to remove the portions of the conductive layer 232 on tops of the mask layer 104 and those between every two columns of pillars 100 first. The conductive layer 232 between the pillars 110 of the same column is not etched because of the protection of the mask layer 234. The anisotropic etching process is continued until the height of the conductive layer 232 on the sidewalls of the pillars 100 is reduced to a predetermined level. The remaining spacer-like conductive layer 232 on the sidewall of each pillar 110 serves as a gate 232a. The gates 232a on the sidewalls of the pillars 100 in one column are connected via the conductive layer 232 between the pillars 110 of the same column, which is protected by the mask layer 234 in the anisotropic etching process, to be a gate line 232a. The gate line 232a can directly serve as a word line. However, another low-resistance conductive line can be further formed overlying and electrically connecting with the gate line to reduce the

resistance.

[0049] Moreover, in the two methods for forming a gate structure around each pillar, some modifications or variations on, for example, the material and the fabrication method of each layer and the fabrication sequence of the layers, are also possible within the scope of this invention.

[0050] Fabrication of Source/Drain

[0051] Referring to FIG. 11, the spaces between the pillars 110 are filled up with an insulating layer 138, which is formed with a material such as silicon oxide and is formed by, for example, performing a plasma-enhanced chemical vapor deposition (PECVD) process and a chemical mechanical polishing (CMP) process in sequence.

[0052] Referring to FIG. 12, the patterned mask layer 104, the pad oxide layer 102, a portion of the mask spacers 134 and a portion of the insulating layer 138 are removed. The four parts may be removed by performing a chemical mechanical polishing (CMP) process, for example, so that the top surfaces of the mask spacers 134 and the insulating layer 138 are substantially coplanar with those of the semiconductor pillars 110. An ion implantation 140 is then conducted to form a doped region 142 in the top portion of each semiconductor pillar 110 to serve as a

source/drain region. The doped region 142 may be an N^+-doped region implanted with phosphorous ions or arsenic ions. A high-temperature annealing process is then performed to repair the damaged lattices in the semiconductor pillars 110 caused by the ion implantation 140, and to drive some dopants from the upper electrode 126 into the sidewall of each semiconductor pillar 110 to form a doped region 144. The doped regions 142 and 144, the gate 132a and the gate insulating layer 130 together form a vertical transistor 145. It is noted that although the doped region 144 is not illustrated in previous figures, the doped region 144 actually grows more or less during every thermal process after the top portion 122 (FIG. 6) of the upper electrode 126 is formed. However, in the preferred embodiment, the doped region 144 grows mainly during the high-temperature annealing process after the doped regions 142 are formed.

[0053] *Fabrication of Bit Lines and Word Lines*

[0054] FIGs. 13-14 illustrate the step of forming the bit lines of the memory array, wherein FIG. 14 is a top view of the resulting structure after the following steps, and FIG. 13 is a cross-sectional view of the resulting structure in FIG. 14 along line XIII-XIII". After the fabrication of the vertical

transistor 145 is completed, bit lines 146 are formed over the substrate 100, wherein each bit line 146 directly contacts with the doped regions 142 in the top portions of the pillars 110 in one row. The bit lines 146 are formed with a material such as N^+-doped polysilicon, and can be formed by using a deposition-patterning method or a damascene method. In addition, a cap layer 1461 can be disposed on each bit line 146, and a protective spacer 1462 can be formed on the sidewalls of each pair of bit line 146 and cap layer 1461 if the bit lines 146 and the cap layers 1461 are formed with a deposition-patterning procedure. The cap layers 1461 and the protective spacers 1462, which are preferably constituted of silicon nitride, are formed to prevent the bit lines 146 from being exposed during the subsequent contact hole etching process, so that the contact holes will be formed in a self-aligned manner. Thereafter, an insulating layer 148 is formed over the substrate 100 covering the bit lines 146 and filling up the gap between every two bit lines 146 to isolate the bit lines 146 from the word lines that will be formed in the next step.

[0055] FIGs. 15-16(a)/(b) illustrate the step of forming additional word lines of the memory array to electrically connect with

the gate lines formed previously. FIG. 15 is a top view of the resulting structure after the following steps, and FIGs. 16(a) and 16(b) are cross-sectional views of the resulting structure in FIG. 15 along line A-A" and line B-B", respectively. After the insulating layer 148 is formed, word lines 150 are formed over the substrate 100, wherein each word line 150 is electrically connected to the gates 132a on the sidewalls of the pillars 110 in one column via at least one contact 152. The contact 152 directly contacts with the conductive layer 132a connecting between two gates 132a on the sidewalls of two adjacent pillars 110 in the same column. The contact 152 and the word line 150 are formed by, for example, forming a contact hole in the insulating layer 148 exposing a portion of the conductive layer 132a, depositing a conductive layer covering the insulating layer 148 and filling up the contact hole, and then patterning the conductive layer. Alternatively, the contact 152 and the word line 150 can be formed with a damascene process.

[0056] Referring to FIGs. 15 and 16(a)/(b), since the capacitor 127 in a DRAM cell of this invention is formed around a semiconductor pillar 110, but not in a deep trench, the trench-filling problem in the prior art caused by high as-

pect ratios of deep trenches does not exist. Meanwhile, the surface area of the capacitor 127 is quite large since the capacitor 127 is formed on four sides of the pillar 110.

[0057] Moreover, since the transistor 145 of a DRAM cell of this invention is formed with a vertical structure, the size of each memory cell can be significantly reduced to remarkably increase the integration of the memory array.

[0058] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.